REMARKS

Claims 1-25 are pending. Applicants acknowledge withdrawal of all previous objections and rejections.

§ 112 Rejections

According to the Office Action, Claims 1-25 are rejected under 35 U.S.C. § 112, first paragraph, allegedly for failing to comply with the written description requirement. Applicants respectfully traverse.

In preface to the remarks provided further below, please note the following.

Per MPEP § 2163.02 (emphases added):

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> The courts have described the essential question to be addressed in a description requirement issue in a variety of ways. An objective standard for determining compliance with the written description requirement is, "does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed." *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). Under *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991), to satisfy the written description requirement, an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and that the invention, in that context, is whatever is now claimed. The test for sufficiency of support in a parent application is whether the disclosure of the application relied upon "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." *Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting *In re Kaslow*, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983)).

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The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement. If a claim is amended to include subject matter, limitations, or terminology not present in the application as filed, involving a departure from, addition to, or deletion from the disclosure of the application as filed, the examiner should conclude that the claimed subject matter is not described in that application.

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Per MPEP § 2163.I.B (emphasis added):

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While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure.

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Per MPEP § 2163.07(a) (emphases added):

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By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter. *In re Reynolds*, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); *In re Smythe*, 480 F. 2d 1376, 178 USPQ 279 (CCPA 1973).

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Considering the above, and in view of the following remarks, Applicants submit that Claims 1-25 satisfy the written description requirement. Specifically, as will be seen from the discussion below, Applicants submit that the application adequately supports: "the accesses form a stream-type sequential access pattern having a direction that is tracked by setting bits in a bit vector" as recited in independent Claim 1; "a sequential access pattern comprising an order in which adjacent storage locations in the first memory are accessed, wherein the order is tracked by setting bits in a bit vector" as recited in independent Claim 9; "using bit vectors to track multiple stream-type sequential access patterns by the processor to the first memory, wherein the access patterns comprise orders in which adjacent storage locations in the first memory are accessed, wherein the orders are tracked by setting bits in respective bit vectors" as recited in independent Claim 18; and "means for using bit vectors to track multiple stream-type sequential access patterns by the processor to the first memory, wherein the access patterns comprise orders in which adjacent storage locations in the first memory are accessed, wherein the orders are tracked by setting bits in respective bit vectors" as recited in independent Claim 22.

First, subject matter with the scope of the term "bit vectors" is disclosed throughout the instant application.

Also, page 8 (lines 8-11) of the application describes "sequentially adjacent locations (e.g., following locations that are directly next to preceding locations) … consecutive locations." Applicants submit that accepted definitions and uses of terms such as "following" and "preceding" implicitly and inherently, if not explicitly, connote "direction" and "order," particularly when used in the context of adjacent or consecutive locations.

Furthermore, page 9 (lines 6-17) of the application describes how access patterns can be observed and recognized. Access patterns can include stream-type sequential access patterns, which in turn can include sequential incrementing patterns and sequential decrementing patterns. For example, a sequential incrementing patterns "show an access to cache line x, then x+1, x+2, and so on. Observations of such sequential accesses enable the intelligent prefetch of subsequent cache lines (e.g., x+3, and so on)" (emphases added). Applicants submit that accepted definitions and uses of terms such as "then" and "subsequent" implicitly and inherently, if not explicitly, connote "direction" and "order," particularly when used in the context of adjacent or consecutive locations.

Page 9 (lines 19-26) of the application describes "a tracker is used to track accesses to a corresponding memory block … each tracker can be used to observe and detect stream-type access patterns … The trackers thus indicate, or predict, which 'target' cache lines should be prefetched" (emphasis added). Applicants submit that accepted definitions and uses of terms such as "detect," "track," and "tracking" implicitly and inherently, if not explicitly, connote "observe the progress of."

Page 11 (lines 5-8) of the application describes "[w]hen the cache line is accessed by the CPU, the decoder 450 sets its indicator accordingly (e.g., sets an indicator bit to one), thereby notifying the prefetcher. In this manner, the indicators 431-446 form a bit vector that is used to predict target cache lines for prefetching" (emphasis added). An example of how a bit vector is formed is described on pages 10 (starting at line 24) and 11 (ending at line 8). Page 11 (lines 10-21) describes an example of how, when the bit vector is formed, a sequential incrementing stream-type access or a sequential decrementing stream-type access can be recognized.

Page 11 (lines 19-21) of the application describes "by tracking accesses to the cache lines …, the trackers indicate target cache lines for predictive loading into the prefetch cache" (emphasis added).

Thus, Applicants submit, in light of the material recited above as well as the application as a whole, and considering how the application would be read and understood by a person of ordinary skill in the art, that the application adequately supports: "the accesses form a stream-type sequential access pattern having a direction that is tracked by setting bits in a bit vector" as recited in independent Claim 1; "a sequential access pattern comprising an order in which adjacent storage locations in the first memory are accessed, wherein the order is tracked by setting bits in a bit vector" as recited in independent Claim 9; "using bit vectors to track multiple stream-type sequential access patterns by the processor to the first memory, wherein the access patterns comprise orders in which adjacent storage locations in the first memory are accessed, wherein the orders are tracked by setting bits in respective bit vectors" as recited in independent Claim 18; and "means for using bit vectors to track multiple stream-type sequential access patterns by the processor to the first memory, wherein the access patterns comprise orders in which adjacent storage locations in the first memory are accessed, wherein the orders are tracked by setting bits in respective bit vectors" as recited in independent Claim 22.

Applicants respectfully assert that the application – expressly, implicitly, and/or inherently – conveys with reasonable clarity to a person of ordinary skill in the art that the Applicants were in possession of what is claimed. In the opinion of the Applicants, the claims do not include subject matter, limitations, or terminology not present in the

application as filed and do not involve a departure from, addition to, or deletion from the disclosure of the application as filed, and the claimed subject matter is supported by the application.

For any or all of the reasons above, Applicants respectfully submit that the basis for rejecting Claims 1-25 under 35 U.S.C. § 112, first paragraph, allegedly for failing to comply with the written description requirement, is traversed.

Conclusions

In light of the above, Applicants respectfully request reconsideration of the rejected claims. Applicants respectfully assert that Claims 1-25 overcome the rejections of record and respectfully solicit allowance of those claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Dated: 2-16-2011

/William A. Zarbis/

William A. Zarbis
Registration No. 46,120
Address: Two North Market Street, Third Floor
San Jose, CA 95113
Phone: (408) 938-9080 Ext. 113